SUB D. 7 C3 cont.

1. (TWICE AMENDED) A stacked-gate flash memory cell having a floating Poly-Si gate with multiply connected surfaces of different shapes comprising:

a semiconductor substrate;

a floating Poly-Si gate with multiply connected top surface having regions of different cross-sectional shapes, said Poly-Si gate having a flat bottom surface;

wherein said cross-sectional shapes are selected from a group consisting of rectangular and triangular shapes;

a conformal inter-poly dielectric layer replicating said shapes over said floating Poly-Si gate; and

a conformal Poly-Si control gate replicating said shapes over said inter-poly dielectric layer.

REMARKS

Claims 1-3 and claims 5, 6 remain in this application. Claim 1 has been twice amended, claim 3 once amended, and claim 4 cancelled.